REMARKS

Reconsideration of this application is respectfully requested in view of the amendments and arguments presented herein. Claims 1-61 remain pending in the present application. Claims 61 has been added. No new matter has been added. Applicant understands that the objections to the drawings and the rejection under 35 U.S.C. 112, second paragraph have been overcome.

35 U.S.C. Section 103(a) Rejections

The present Office Action rejects Claims 1-5, 7-14, 18-19, 21-32, 38-41, 47-53 and 56-59 as being unpatentable over US Patent No. 5,202,987 (hereinafter Bayer) in view of US Patent No. 5,504,670 (hereinafter Barth). Applicant respectfully traverses.

Applicant directs the Examiner to Claim 1 which recites (emphasis added):

> A resource management and task allocation controller for a multicore processor having a plurality of interconnected processor elements, at least one of which is a master processing unit, each element providing resources for processing executable transactions, the controller being in communication with each of the processor elements but separate from the master processing unit, and comprising control logic to allocate executable transactions within the multicore processor to a one of the processor elements in accordance with one of a range of pre-defined allocation parameters.

Claims 21 and 38 recite distinguishing limitations similar to those of Claim 1.

The response to arguments section alleges that Bayer teaches a multiprocessor system (multicore) with plurality of interconnected processor elements (processor) where each processor provides resources for processing executable transaction. Applicant respectfully disagrees. Applicant points out that it appears the rejection is inappropriately equating a multiprocessor system to a multicore processor. Applicant respectfully asserts that Bayer in combination with Barth does not teach or suggest a multicore processor nor a controller of a multicore processor, as claimed. For example, Applicant points out that a multicore processor may include multiple processors or processing elements on a single chip or integrated circuit (IC). As a further example, Applicant points out that a multicore processor may include dissimilar processing elements. Applicant can find no mention of a multicore processor in either of Bayer or Barth.

Applicant respectfully asserts that Barth does not remedy the shortcomings of Bayer. To the extent that Barth may mention that in a multi-site tester, one processor controls the testing operation for all the sites and acts as a master (Col. 2, lines 24-26), Applicant respectfully asserts that Barth does not teach or suggest a master processor of a multicore processor

(emphasis added). Applicant points out that Barth mentions that with multi-site testers, multiple ICs may be tested at the same time by placing each IC in a different site (Col. 2, lines 7-8). Therefore, Applicant understands the processor controlling the testing for the sites in Barth to control multiple ICs in different semiconductor packages. For the reasons stated above, Applicant understands processors in different semiconductor packages to be substantially different from a multicore processor, as claimed. Therefore, Applicant respectfully asserts that Barth does not teach a master processing unit in a multicore processor, as claimed. Thus, Applicant respectfully asserts that the combination of Bayer and Barth does not teach or suggest a multicore processor or controller in a multicore processor, as claimed.

Further, Applicant respectfully asserts that the combination of Bayer and Barth does not teach or suggest a controller being separate from a master processor. The rejection admits that Bayer does not specifically disclose at least one of the processing units being a master processing unit. Applicant points out that that Barth mentions that one processor acts as the master for the control system (Col. 2, lines 25-26) and further mentions that the master processor controls the testing operation for all the sites or ICs (Col. 2, 24-25). That is, Applicant understands Barth to mention a master processor acting as a controller. Therefore, Applicant respectfully asserts that Barth does not teach a controller separate from the master processing

unit, as claimed (emphasis added). Similarly, Applicant respectfully asserts that Barth cannot teach a controller separate from a master processing unit because Barth does not teach or suggest a master processor. Therefore, Applicant respectfully asserts that embodiments of the present invention as recited by Claim 1 are not rendered obvious by the combination of Bayer and Barth within the meaning of 35 U.S.C. 103(a).

Independent Claims 21 and 38 are patentable for similar reasons as recited above. Accordingly, Applicant respectfully asserts that dependent Claims 2-5, 7-14, 18-19, 22-32, 39-41, 47-53, and 56-59 are patentable by virtue of their dependency.

As per Claim 26, the rejection alleges that Bayer teaches the dedicated memory being accessible by both the controller and by at least one further component of the multicore processor. Applicant respectfully disagrees. As mentioned above, Applicant respectfully asserts that Bayer does not teach or suggest a multicore processor. To the extent that Bayer may mention that each RAM word is divided into three sections, A, B and C, each of them having a separate external access (Col. 22, lines 11-12), Applicant respectfully assert that Bayer does not teach or suggest that the memory is accessible by at least one further component of a multicore processor, as claimed. That is, Applicant respectfully asserts that the mere mention of

external access does not teach or suggest the object that is using the external access. Therefore, Applicant respectfully asserts that embodiments of the present invention as recited in Claim 26 are not rendered obvious within the meaning of the 35 U.S.C. 103(a).

As per Claim 49, the response to arguments section alleges that Barth teaches creating the system for program execution based on the user requirements and needs which specifies the executable program parameters on the system. Applicant respectfully disagrees. To the extent that Barth may mention that the actual number of processors in the computer system is a design choice dependent on the requirements of the manufacturer and the needs of the user (Col. 4, lines 1-4), Applicant respectfully asserts that Barth does not teach or suggest the limitations of the set of scheduling parameters being user-definable, as claimed (emphasis added). That is, Applicant respectfully asserts that the number of processors being based on the needs of a user is substantially different from a user defined set of scheduling parameters, as claimed (emphasis added). Therefore, Applicant respectfully asserts that embodiments of the present invention as recited in Claim 49 are not rendered obvious within the meaning of the 35 U.S.C. 103(a).

The present Office Action rejects Claims 6, 20, 33-37, 45, and 46 as being unpatentable over Bayer in view of Barth and further yet in view of US Patent No. 6,314,501 (hereinafter Gulick). Applicant respectfully traverses.

For the reasons stated above, Applicant respectfully submits that independent Claim 1, from which Claims 6 and 20 depend and independent Claim 21, from which Claims 33-37 depend, and independent Claim 38, from which Claims 45 and 46 depend are allowable over Bayer in view of Barth. In addition, Applicant respectfully submits that Gulick does not remedy the shortcomings of the combination of Bayer in view of Barth. Therefore, Applicant respectfully submits that Claims 6, 20, 33-37, 45, and 46 are also allowable over the combination of Bayer, Barth, and Gulick as being dependent on allowable base claims.

As per Claim 20, the response to arguments section alleges Gulick teaches having core services software that accommodates inter-processor communication and creates (converts) signal based on received signals from a sending client to a receiving client and further alleges that cores services software gathers information from the request sending client and builds (converts) a signal for the receiving client to be able to process the request. Applicant respectfully disagrees. To the extent that Gulick may mention an inter-processor interrupt mechanism and the core services software on the

sending partition generates an inter-processor interrupt to one of the processors of the receiving partition (Col. 45, lines 44-55), Applicant respectfully asserts that Gulick does not teach or suggest converting from system interrupts in a format employed with the multicore processor into controller interrupts in a second format, as claimed (emphasis added). That is, Applicant points out that the mere mention of receiving an interrupt signal and sending an interrupt signal by Gulick does not teach or suggest converting the interrupt signal. Further, Applicant understands to Gulick to mention interrupts between processors. In constrast, Applicant does not understand Guilick to mention converting system interrupts into controller interrupts, as claimed (emphasis added). Therefore, Applicant respectfully asserts that embodiments of the present invention as recited in Claim 20 are not rendered obvious within the meaning of the 35 U.S.C. 103(a).

The present Office Action rejects Claims 43 and 44 as being unpatentable over Bayer in view of Barth further yet in view of US Patent 5,592,671 (hereinafter Hirayama) and further yet still in view of Gulick. Applicant respectfully traverses.

For the reasons stated above, Applicant respectfully submits that independent Claim 38, from which Claims 43 and 44 depend are allowable over Bayer in view of Barth in further in view of Gulick. In addition,

Applicant respectfully submits that Hirayama does not remedy the shortcomings of Bayer in view of Barth in further view of Gulick. Therefore, Applicant respectfully submits that Claims 43 and 44 are also allowable over the combination of Bayer, Barth, Hirayama, and Gulick as being dependent on allowable base claims.

CONCLUSION

Applicant respectfully asserts that all claims (Claims 1-60) are in condition for allowance and Applicant earnestly solicits such action from the Examiner. The Examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,
MURABITO, HAO & BARNES

Dated: 3/4, 2009

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